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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,969	04/03/2001	Ichiro Kumata	450100-03123	1867

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EXAMINER	
WILLIAMS, LAWRENCE B	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 08/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/824,969	KUMATA, ICHIRO	
	Examiner	Art Unit	
	Lawrence B Williams	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,10,11,16,17 and 25* is/are rejected.

7)☒ Claim(s) *2-9,12-15 and 18-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 April 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because:

a.) Examiner suggests applicant add an "s" to transmit in line 11.

b.) Examiner suggests applicant replace "twice" with "two" in line 16.

c.) Examiner suggests applicant delete the word "out " in line 17.

d.) Examiner suggests applicant delete the letter "a" after from or use the word "line" in singular form.

Correction is required. See MPEP § 608.01(b).

2. The disclosure is objected to because of the following informalities:

a.) Examiner suggests applicant rewrite lines 1-4, beginning with "and" on page 50 for clarification purposes.

b.) Examiner suggests applicant rewrite lines 9-14 of page 42 for clarification purposes.

Appropriate correction is required.

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 10-11, 16-17 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Calvignac et al. (US Patent RE34896).

(1) With regard to claim 1, Calvignac et al. discloses in Figs. 2 and 12 a transmitting circuit comprising a clock signal transmitting circuit (5) for transmitting a clock signal through a first signal line (9); a synchronization data generating circuit (5) for generating synchronization delimiter of serial data being transmitted of a predetermined unit length, and whose value changes two or more times in a predetermined time interval associated with the clock signal; and a data transmitting circuit for superposing the data on each serial data of the generated synchronization unit length and for synchronizing the serial data with the clock signal and transmitting the serial data through a second signal line (7). (col. 9, lines 12-36). Calvignac et al. uses a variable delimitation pattern controlled by a clock signal. This variable delimiter pattern has a predetermined unit length control by the clock signal dependent upon the data speed and would inherently change value "two or more times" dependent upon the data rate of the intended user.

(2) With regard to claim 9, Calvignac et al. also discloses in Fig. 2, a transmitting circuit as set forth in claim 1, further comprising a parallel-serial converting circuit (5) for converting parallel data being transmitted to serial data (LIC; 11-1-8), wherein said synchronization data

generating circuit generates of the converted serial data of a predetermined unit synchronization data representing a delimiter length; said data transmitting circuit transmits the converted serial data (col. 3, lines 12-21).

(3) With regard to claim 10, claim 10 inherits all limitations of claim 1 above as claim 10 merely discloses the method involved in the transmitting circuit of claim 1.

(4) With regard to claim 11, Calvignac et al. discloses in Figs. 7, 8 and 12, a receiving circuit comprising a clock signal receiving circuit for receiving a clock signal transmitted through a first signal line; a serial data receiving circuit for receiving serial data synchronized with the clock signal and transmitted through a second signal line; a synchronization data detection circuit for detecting data from the received serial data and using the same as synchronization data, said data changing its value two or more times within a predetermined period received clock signal; and associated with the a data processing circuit for detecting the predetermined unit length of the received serial data by using the detected synchronization data as a delimiter (col. 19, line22- col. 20., line 66).

(5) With regard to claim 12, Calvignac et al. also discloses in Figs.10 and 12, a receiving circuit as set forth in claim 11, wherein said data processing circuit (246, deserializer) converts said received serial data of said detected predetermined unit length to parallel data.

(6) With regard to claim 16, claim 16 inherits all limitations of claim 11 above as claim 16 merely discloses the method involved in the receiving circuit of claim 11.

(7) With regard to claim 17, claim 17 inherits all limitations of claims 1 and 10 and the transmitting and receiving circuits as disclose in these claims disclose the data communication apparatus as disclosed in claim 17.

(8) With regard to claim 25, claim 25 inherits all limitations of claim17. Furthermore, Calvignac et al. also discloses in Figs. 2, 10, and 12, a data communication apparatus as set forth in claim 17, the transmitting circuit further comprising a parallel-serial converting circuit (246, deserializer) for converting parallel data being transmitted to serial data, wherein the synchronization data generating circuit of the transmitting circuit generates synchronization data representing a delimiter of the converted serial data of a predetermined unit length; the data transmitting circuit of the transmitting circuit transmits the converted serial data, the data processing circuit of said receiving circuit converts said received serial data of said detected predetermined unit length to parallel data.

Allowable Subject Matter

6. Claims 2-9, 12-15, 18-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 703-305-6969. The examiner can normally be reached on Monday-Friday (8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence B. Williams

lbw
July 30, 2004

STEPHEN CHIN
SUPERVISORY PATENT EXAMINE
TECHNOLOGY CENTER 2600